Tennessee Tech UNIVERSITY

Time-Reversal Based Range Extension Technique for Ultra-wideband (UWB) Sensors and Applications in Tactical Communications and Networking

Technical Report (Quarterly)

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This technical report (quarterly) details the work for Office of Naval Research (ONR) by Tennessee Tech. The goal of this project—jointly funded by ONR, NSF, and ARO—is to build a general purpose testbed with time reversal capability at the transmitter side. The envisioned application is for UWB sensors and tactical communications in RF harsh environments where multipath is rich and can be exploited through the use of time reversal.
In the past quarter, we focus on rethinking about the role of the radio test-bed and on preparing for improving the test-bed. Bit rate scalability is preferred for reliable transmission in different channel conditions. To transmit over a longer distance, current bit rate of 6.35 Mb/s is too high.

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Executive Summary

This technical report (quarterly) details the work for Office of Naval Research (ONR) by Tennessee Tech. The goal of this project—jointly funded by ONR, NSF, and ARO—is to build a general purpose testbed with time reversal capability at the transmitter side. The envisioned application is for UWB sensors and tactical communications in RF harsh environments where multipath is rich and can be exploited through the use of time reversal.

In the past quarter, we focus on rethinking about the role of the radio test-bed and on preparing for improving the test-bed. Bit rate scalability is preferred for reliable transmission in different channel conditions. To transmit over a longer distance, current bit rate of 6.35 Mb/s is too high.

One challenge associated with extended range of transmission is reliable synchronization when received signal is very weak. A robust synchronization scheme should be designed and implemented. Achieving a wide range of bit rates is mainly in base band design and digital implementation aspects. A hardware preparation is to change receiver-side FPGA from the Virtex 2 version to Virtex 5 version. Our tentative goal is to increase the indoor transmission range to 15 meters at bit rates of sub-mega bits per second.

Contents

Chapter 1

Introduction

The over-the-air demonstration of the concept of time reversal for a ultra-wideband radio has been achieved recently in our Lab. In particular, synchronization has been obtained over the air. This even is, indeed, a landmark in the development of UWB radios.

In the past quarter, we focus on rethinking about the role of the radio test-bed and on preparing for improving the test-bed. Bit rate scalability is preferred for reliable transmission in different channel conditions. To transmit over a longer distance, current bit rate of 6.35 Mb/s is too high. One challenge associated with extended range of transmission is reliable synchronization when received signal is very weak. A robust synchronization scheme should be designed and implemented. Achieving a wide range of bit rates is mainly in base band design and digital implementation aspects. A hardware preparation is to change receiver-side FPGA from the Virtex 2 version to Virtex 5 version. Our tentative goal is to increase the indoor transmission range to 15 meters at bit rates of sub-mega bits per second.

In addition to the bit rate issue, improving the RF front-ends and the mixed-signal sections have been considered, too. The current RF front-ends have some limitations that prevent from being further explored. These limitations include fixed center frequency and less dynamic range. In the mixed-signal sections, connection between an FPGA and an ADC (or DAC) is still a bottleneck that restricts the system performance. These issues are covered in this report. The fundamental limit with respect to transmitter-side preprocessing has been studied in parallel with our implementation work. Some new theoretical results are presented in this report as well.

Long term wise, this radio test-bed will evolute to a general purpose experimental platform. In particular, our test-bed is in a unique position to be converted to wideband cognitive radio test-bed. Anti-jamming can be easily included, too.

For cognitive radio, wideband spectrum sensing is the bottleneck. Time reversal combined with dynamic spectrum access will add enhanced security to the UWB sensor network.

Chapter 2

Bit Rate Scalability

Currently the chip rate is 25 Mcps and it seems appropriate for a short transmission range. For ranges over 10 m in indoor environments, the chip rate of 25 Mcps, corresponding to a pulse repetition interval 40 ns, can lead to inter-pulse interference, because the delay spreads at these propagation ranges are usually over 40 ns. Of course, time reversal pre-filtering can reduce the impact of inter-pulse interference to some extent. We will keep a fixed chip rate and change the bit rate by varying the symbol length in chip. Tentatively, a lowest bit rate 390.625 (=25000/64) kbps is chosen. This bit rate means 64 chips per symbol (bit), and a 16-time (about 12 dB) increase in symbol energy. The current data frame structure includes a payload of 3840 chips. We propose two options for modifying the system.

Option 1: chip rate = 25 Mcps, bit rates = 6.25 Mbps, 1.5625 Mbps, 390.625 kbps;

Option 2: chip rate = 12.5 Mcps, bit rates = 3.125 Mbps, 781.25 kbps, 195.3125 kbps.

These changes will affect the receiver baseband structure. The demodulation process has to match the symbol length. The current synchronization design is questionable at weak-signal burst-mode condition. The synchronization issue is still under study and we will provide a solution soon.

Chapter 3

Receiver FPGA Platform Transplant from Virtex 2 to Virtex 5

3.1 Receiver improvement

At current stage, the test-bed have successfully implemented time-reversal communications,that means the receiver can receive focusing signals both at time and space domain. The transmitter with Xilinx Virtex-5 LXT Prototype Platform provides powerful signal processing capability, which enables the transmitter to generate arbitrary continuous baseband waveform for general purpose of communication or remote sensing. While at the receiver side, Virtex-2 platform was employed as digital back-ends to implement all digital signal processing,such as demodulation and synchronization, but currently for Virtex-2, the logic resources utilization is already up to 70%, besides,the inadequate clock rate and absent DSP core, make it almost impossible to implement any more functions or complex algorithms, so to change the receiver digital back-ends from Virtex-2 platfrom to a more advanced platfrom becomes more and more urgent. On the other hand, energy detection employed in the receiver suffers from performance penalty, when it's necessary to perform coherent reception, a powerful signal processing unit is also a must.

Now, the new FPGA board that are going to be employed is a Xilinxs Virtex-5 LXT Development board, it has a Samtec 100-pin FastDAACS connector, which is capable of supporting a high speed connection up to multi GHz. Fig.3.1 shows its picture. The Virtex-5 family is built upon the industry's most advanced 65-nm triple-oxide technology, breakthrough new ExpressFabric(TM) technology and proven ASMBL(TM) architecture. XC5VLX110T FFG1136 prototype platform was chosen to host our Virtex-5 chip, as shown in Figure 2. The platform is optimized for high-performance logic with low-power serial connectivity and high speed, from 100Mb/s to 3.2 Gb/s, which is needed in our system. Based on this Platform, we will greatly benefit from the following features:

- 550MHz Clock technology, up to 12 DCMs and one PLL; 550MHz, 36 Kbit block RAM/FIFOs would enable our system work at a high speed.
- 1.0V core voltage, 1.2 to 3.3V I/O Operation, the Virtex-5 addresses offera a 35
- Up to 160 x 54 CLBs(Configurable Logic Block) with 1.1 million gates. Such big logic resources match our system's requirements since all base-band processing are to be implemented in FPGA.

- Up to 640 User I/O, each with high performance selectIO technology, can work at 1.2 Gbits/s LVDS (differential pairs) and 800 Mbits/s HSTL & SSTL (single ended). Would enable high-speed connection with other boards and devices, such as high D/A and A/D converter.

- Power-optimized high-speed serial transceiver blocks for enhanced serial connectivity, 100 Mb/s to 3.2 Gb/s, this feature would make huge number data could be downloaded to FPGA at a high speed, since there would be huge estimated channel information need to processed at our digital back-ends.

- Advanced DSP48E slices, featuring 25-bits x 18-bit two's complement multiplier, optional pipeline stages for enhanced performance and optional 48-bit accumulator. This would make it possible to implement complex algorithms with FPGA, for example, synchronization.

Other than the features mentioned above, Virtex-5 have many other advantages, such as Hard-coded PCI Express compliant integrated Endpoint block, ChipSynch - support networking/telecomms interfaces up to 1.25 Gbits/s, Tri-mode 10/100/1000 Mb/s Ethernet MACs. These features allow us to build the highest levels of performance and functionality into FPGA-based systems.

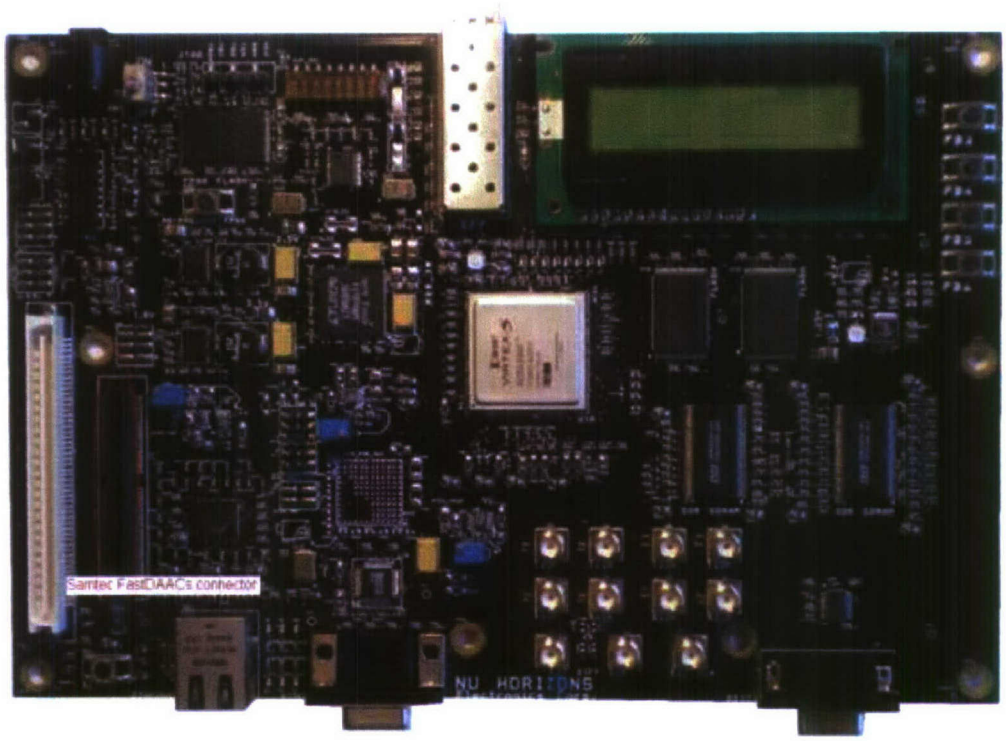


Figure 3.1: Xinlinx Virtex-5 LXT Development Board from Nuhorizons INC.

Besides RF front-end, the receiver improvement includes two parts, one is the the connection between FPGA board and ADC board, the other one is FPGA coding.

3.2 connection board

We are utilizing the MAX108 evaluation board to perform the analog-to-digital conversion in the receiver side, the FPGA board and the ADC board are connected together through 50 Ω SMA cables, with a ADC/FPGA interface board which is plugged into the FPGA development board, The interface solution can support signals with frequency of up to several GHz, which can be shown as Fig. 3.2. Since we need to change the FPGA board, then we have to change the interface board correspondingly.

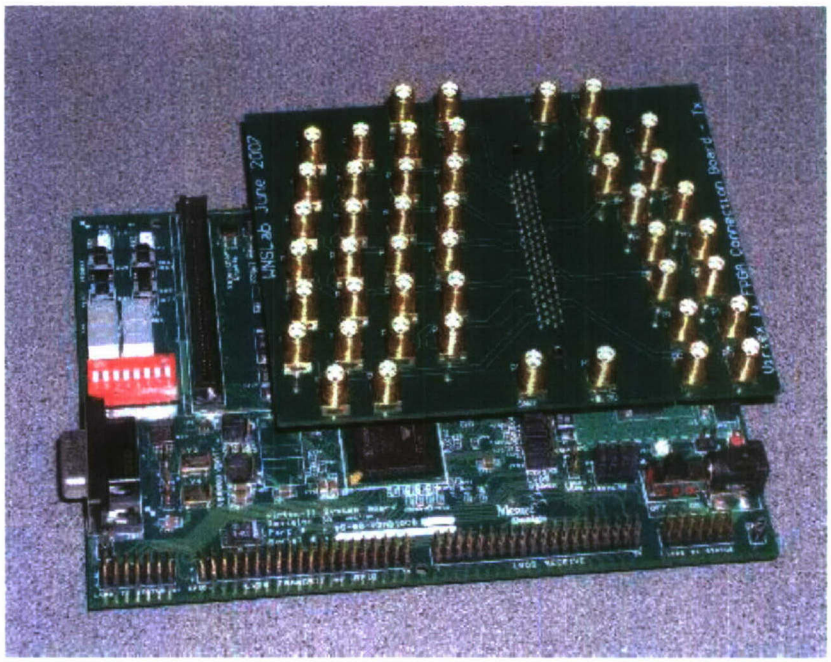


Figure 3.2: Old interface connection between Xinlinx Virtex-2 Board and ADC board

For the design of the high-speed interface between ADC and FPGA, signal integrity has become a critical issue. Many signal integrity problems are electromagnetic phenomena in nature and hence related to the EMI/EMC. There are two concerns for signal integrity: the timing and the quality of the signal.An interface has been carefully designed to solve the signal integrity issue. PCB layout, transmission line terminations, and connection cables are three major considerations in the high speed ADC/FPGA interface design.

A 4-layer PCB board is designed and fabricated to have 50 Ω characteristic impedance for each trace. The PCB layer stack is shown in Fig. 3.3. As shown in Fig. 3.4, for each pair of LVPECL signals, the traces are designed to have same length such that the positive and negative signals experience same delay.

3.3 FPGA coding modification

For FPGA coding, the first change must be made is the pins assignment, Including the the dual 8-bits Maxim ADC data output signals, and the differential clock signals, there are totally 17 pairs of signals that will be fed into FPGA board, however the Samtec connector only have 17 pairs I/O pins and there is no other availble I/o pins on the new

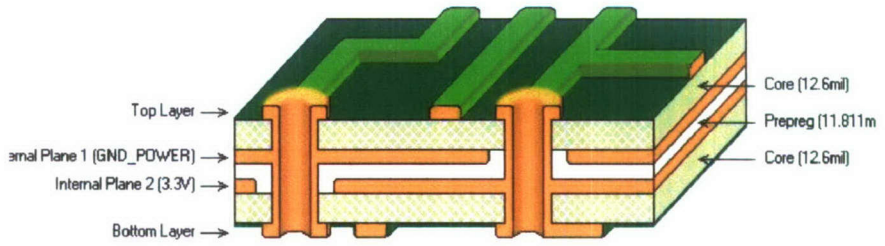


Figure 3.3: New interface board PCB layer stack

board, that means all the I/O pins must be occupied by the input signals, so for the output signals such as output data, synchronization flag, state and value threshold, there will no dedicated I/O pins, our solution is to assign the EXTERNAL GTP clock pin J10 to output data, and for other signals, using Chipscope to view their values. the pins assignment can be shown as Fig. 3.5.

After pins assignment, it comes to the coding modules,whose architecture is shown as Fig. 3.6. For the interface module,it is used to perform three functions: data buffer, data rate conversion and clock domain crossing, its inputs are ADC output data at a speed of 400MHz and outputs are a block of data at 25MHz for digital processing. the modification includes I/O buffers, clock distribution, DDR instantiation and a 64X64 FIFO module.

Clock module provides various clock signals for all the other modules, for Xilinx Virtex-2, DCMs (Digital Clock Manager) are used to generate clock signals, DCM uses matched delay lines to provide precise phase shift, zero clock insertion delay and multiple precise phase outputs (90, 180, 270 degree). While Virtex-5 integrates 550 MHz Clock Technology, providing powerful clock management tile (CMT) clocking, where each CMT contains two DCMs and one PLL/PMCD, compared with DCM, PLL can get the best possible, lowest jitter clock. So for the coding modification, we use PLLs for clock management, which supply a 100MHz clock signal for FIFO module, a 25MHz clock signal for multiple modules for baseband processing.

For integration module, its 32 integrators accumulate the coming signals from interface module over a chip level, and provide information for synchronization, it is simple but involves a lot of computation and requires fast integration, the most important part in this module is the accumulator, thanks to Xilinx Virte-5's advanced DSP48E technology, the integrators can be implemented much more faster. DSP48E slice resources contain a 25 x 18 twos complement multiplier and a 48-bit adder/subtacter/accumulator. Each DSP48E slice also contains extensive cascade capability to efficiently implement high-speed DSP algorithms.

Synchronization module is the most important part in the receiver side, it determines whether the system's working or not. there are two levels of synchronization, chip synchronization and symbol synchronization. In the testbed, 32 integrators are employed to achieve the chip synchronization. The output of the synchronized integrator is sampled at chip rate and sent to a digital correlation with 60 taps for symbol synchronization. Once the chip level synchronization is achieved, the 60 chips OOC can be used to determine the symbol synchronization in the testbed. The detection of the symbol synchronization is based on the correlation between the output of the synchronized integrator and the OOC code. The maximum output of the correlator indicates the symbol synchronization. In order to achieve the initial timing acquisition quickly, a parallel searching is employed instead of a serial searching. The cost of the parallel searching is that more FPGA resources are occupied. A bank of parallel integrators followed by selection of the maximum integrator outputs is implemented in the FPGA device for the chip synchronization. The structure is shown in Fig. 3.7 where Tb is the chip duration, N is the number of integrators. The goal is to find the integrator whose output is the maximum among all integrators. The timing accuracy of the chip synchronization is related

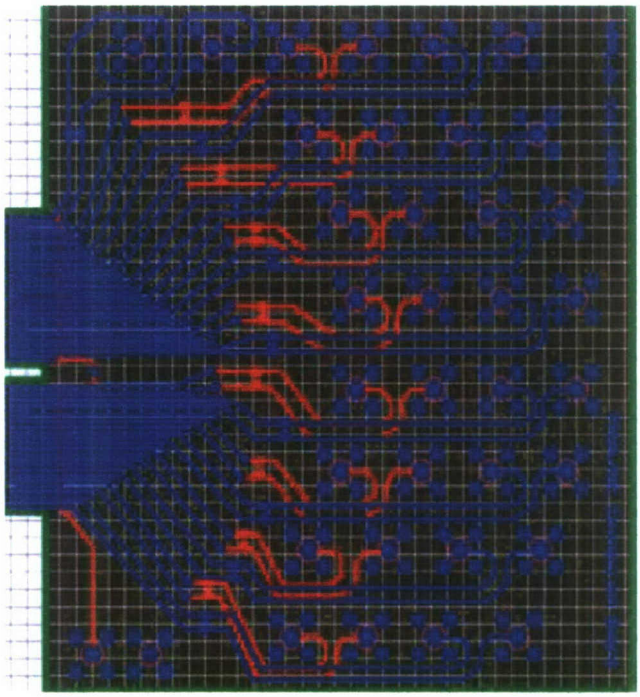


Figure 3.4: Interface board top layer layout

with the number of integrators N. In the testbed, 32 integrators are employed to achieve the chip synchronization. For Xilinx Virtex-5 device, its resources is more than 10 times of Virtex-2 device,so there is great advantage for the integration work as well as for the improvement of synchronization procedure.

For other modules in the testbed such as the finite state machine and decision, there is no modification made, it works the same as in the Virtex-2 device. The design summary and routing diagram are shown in Fig. 3.8 and Fig. 3.9 respectively.

3.4 FPGA timing closure issues

FPGA design sizes have reached unprecedented levels with million gate parts becoming increasingly common, However, the issue of timing closure on the larger and more complex FPGAs has become one of the more daunting for designers to tackle without the right set of tools. The timing closure problem for these high-end FPGAs has its root in the increased net delays in relation to the gate delays. The design size and interconnect issues together have led to an inefficient iterative methodology in completing designs.

For the testbed, timing closure issues exist both in the transmitter side and receiver side. Since transmitter side utilizes less resources and the logic is not as complex as the receiver side, so the timing closure issue is somewhat relaxed. however, in the receiver side, timing closure is critical for its large design size and complex logics, even in the new Virtex-5 FPGA.

Typically, there are global timing constraints, Offset constraints, specific path constraints and groups constraints,

INPUT

CONNECTOR	Pins	Signals		Pins	Signals
	E18	board_clk			
	AD14	rst_sw			
FX2-IO1	D9	REFCLKP	FX2-IO19	C6	RXN_data_P[0]
FX2-IO2	D10	REFCLKN	FX2-IO20	C7	RXP_data_P[0]
FX2-IO3	F8	RXN_data_A[0]	FX2-IO21	B7	RXN_data_P[1]
FX2-IO4	F7	RXP_data_A[0]	FX2-IO22	A7	RXP_data_P[1]
FX2-IO5	G9	RXN_data_A[1]	FX2-IO23	G7	RXN_data_P[2]
FX2-IO6	F9	RXP_data_A[1]	FX2-IO24	H7	RXP_data_P[2]
FX2-IO7	J8	RXN_data_A[2]	FX2-IO25	A5	RXN_data_P[3]
FX2-IO8	H8	RXP_data_A[2]	FX2-IO26	B6	RXP_data_P[3]
FX2-IO9	A8	RXN_data_A[3]	FX2-IO27	A10	RXN_data_P[4]
FX2-IO10	A9	RXP_data_A[3]	FX2-IO28	B10	RXP_data_P[4]
FX2-IO11	E7	RXN_data_A[4]	FX2-IO29	A3	RXN_data_P[5]
FX2-IO12	E8	RXP_data_A[4]	FX2-IO30	A4	RXP_data_P[5]
FX2-IO13	C8	RXN_data_A[5]	FX2-IO31	A12	RXN_data_P[6]
FX2-IO14	B9	RXP_data_A[5]	FX2-IO32	B11	RXP_data_P[6]
FX2-IO15	D6	RXN_data_A[6]	FX2-IO33	B5	RXN_data_P[7]
FX2-IO16	E6	RXP_data_A[6]	FX2-IO34	B4	RXP_data_P[7]
FX2-IO17	D8	RXN_data_A[7]			
FX2-IO18	C9	RXP_data_A[7]			

OUTPUT

GTP		
EXTERNAL GTP CLOCK		
GCLK0(J10)	E13	data_out

Figure 3.5: New pins assignment in the receiver FPGA

for some case, there are area constraints, which enable partitioning of the design into physical regions for mapping, packing, placement, and routing. The timing closure flow can be shown as Fig 3.10. Generally, designs over 50MHz should use timing constraints, while for the testbed, processing rate is up to 400Mhz in the interface module. After applying global timing constraints, if the system meets the timing requirements, then there is no need to add other constraints, otherwise,there is a need to increase place and route effort, if it still fails to meets timing, then we need to find the specific paths and add critical path constraints, after that, we may need to run multi-pass place and route, further, we may also need to do some floorplan work. For special cases, area constraints may be employed. If all these strategies still can't meet timing closure requirements, then the only solution is to go back to start over and rewrite the codes.

In the testbed, we add global timing constraints, offset constraints, and multiple group constraints for almost each modules, Finally, the timing report is shown as Fig 3.11, the timing works fine.

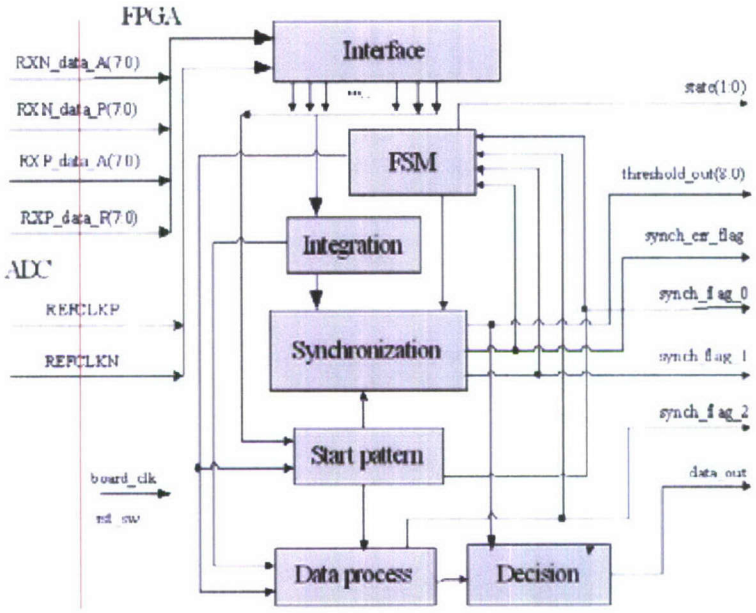


Figure 3.6: The functional diagram of receiver baseband

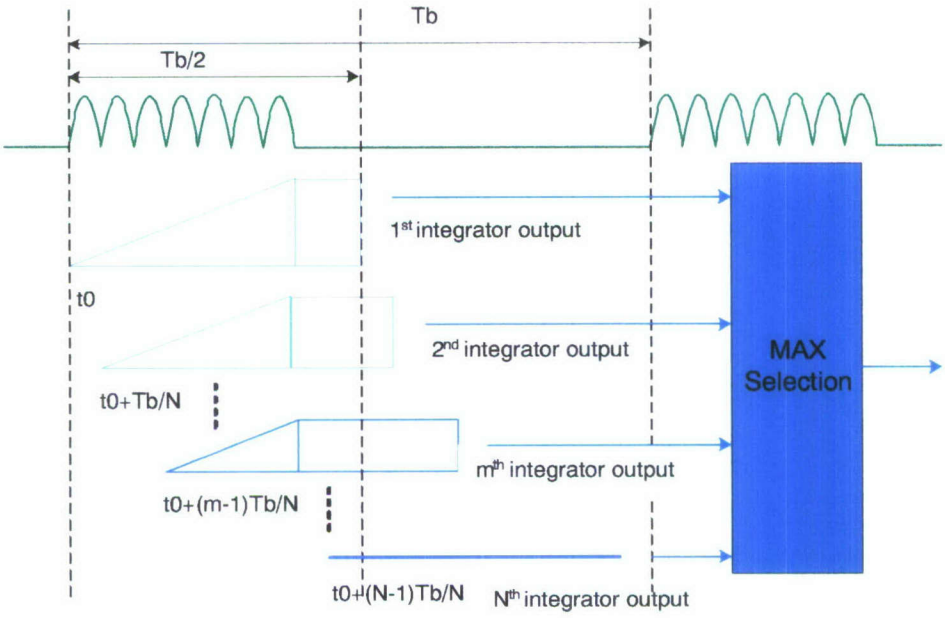


Figure 3.7: Chip level synchronization

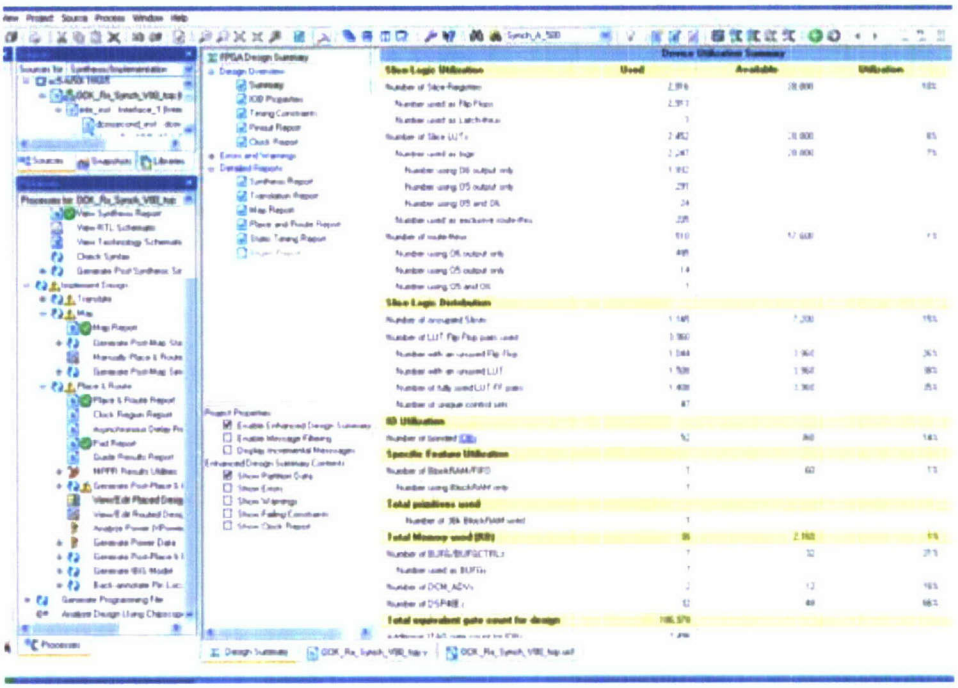


Figure 3.8: Receiver FPGA design summary

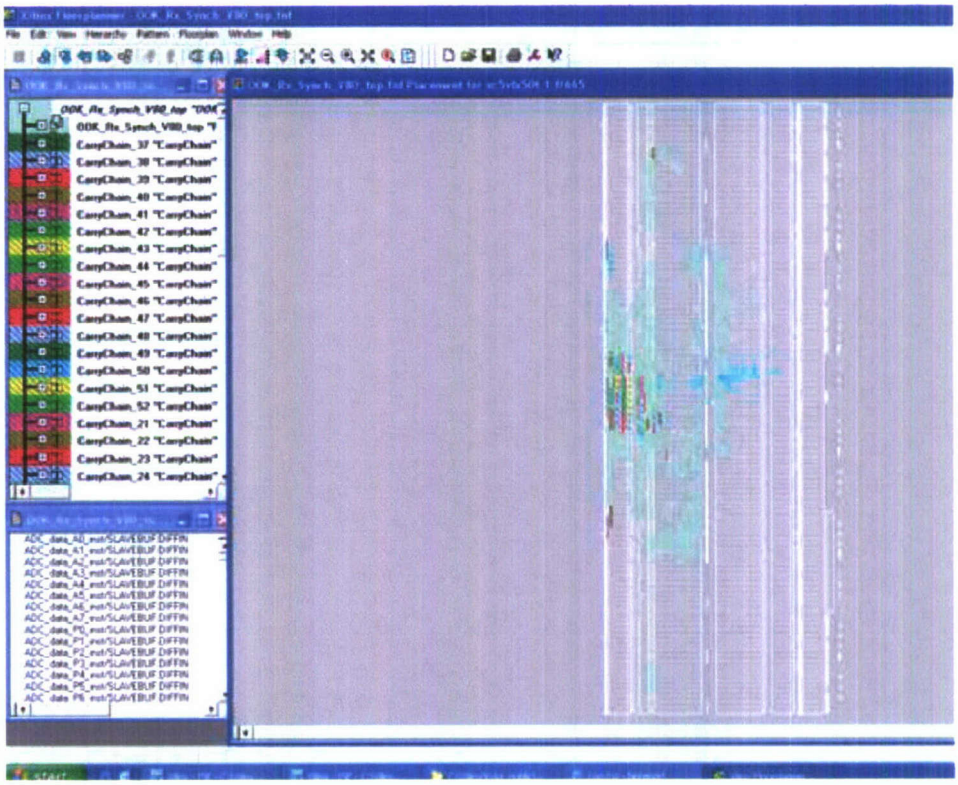


Figure 3.9: Receiver FPGA routing diagram

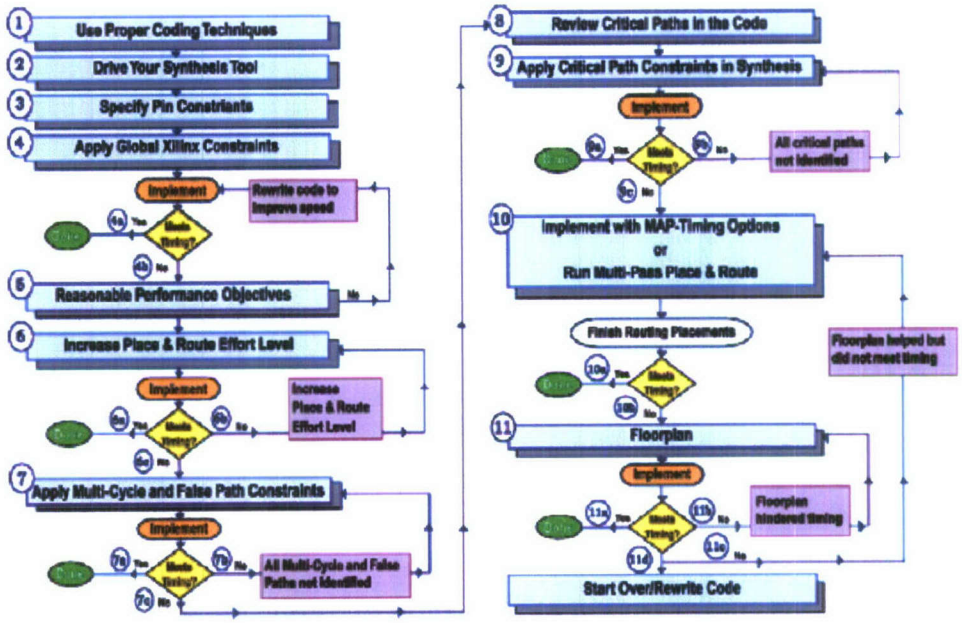


Figure 3.10: Xilinx FPGA timing closure flow

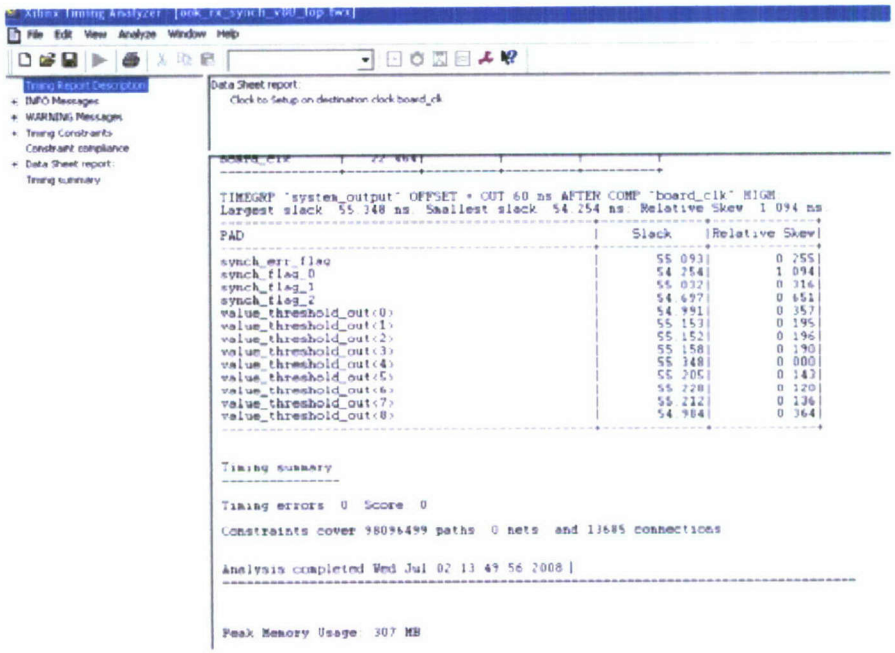


Figure 3.11: Receiver FPGA timing report

Chapter 4

Achieving Variable Center Frequency: Selection of Local Oscillators

4.1 Introduction

One potential evolution for our current test-bed is to be a wideband cognitive radio system. To achieve this goal, we only need to add a spectrum scanning module and change the RF part, while the baseband processing can be handled by our current FPGA platform.

The novel characteristic of cognitive radio transceiver is a wideband sensing capability of the RF front-end. This function is mainly related to RF hardware technologies such as wideband antenna, power amplifier, automatic gain controller (AGC) and local oscillator(LO). RF hardware for the cognitive radio should be capable of tuning to any part of a large range of frequency spectrum. Also such spectrum sensing enables real-time measurements of spectrum information from radio environment. Figure 4.1 shows a typical architecture of wideband RF/analog front-end.

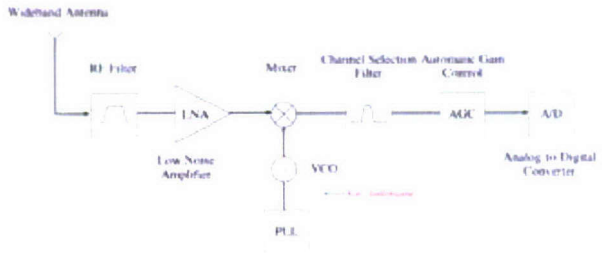


Figure 4.1: The architecture of cognitive radio wideband RF analog front-end.

In wideband systems such as the UWB cognitive radio system, proper LO signal generation is the most challenging issue in RF front-end because it must cover a wide frequency range and consume very little power in doing it, as well as switch its frequency at a very fast speed.

In order to address this RF agility challenge and get ready to develop our next generation test-bed, Selection of proper LO is being carried out to achieving variable venter Frequency

4.2 VCO and PLL

A LO mainly consists of a VCO and a precise Phase locked loop (PLL). Figure 4.2 shows the architecture of a standard PLL based frequency synthesizer.

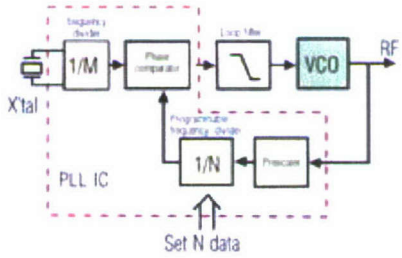


Figure 4.2: The diagram of PLL based frequency synthesizer.

VCO: The VCO generates a signal at a specific frequency for a given voltage to mix with the incoming signal. This procedure converts the incoming signal to baseband or an intermediate frequency.

Wideband VCOs are used in a variety of RF and microwave systems, including broadband measurement equipment, wireless and TV applications and military electronic countermeasures (ECM) systems. In modern ECM systems, they serve as the frequency-agile local oscillators in receiver subsystems and fast-modulation noise sources in active jamming subsystems. Among wideband tunable signal sources such as YIG-tuned oscillators, wideband VCOs are preferable because of their small size, low weight, high settling time speed and capability of fully monolithic integration. Therefore, modern radar and communication applications demand VCOs that are capable of being swept across a wide range of potential threat frequencies with a speed and settling time far beyond those of the YIG-tuned oscillators.

In spectrum sensing, frequency-hopping synthesizer requires very fast frequency switching time. One can build several VCOs and dividers to generate all the required tones; however, it may dissipate a lot of power. Another approach is to utilize single-sideband mixers. This approach may produce all the frequency tones by using one or two synthesizers. However, the traditional single-sideband mixers dissipate much power and usually suffer from spurious spectrum purity.

PLL: The PLL ensures that a signal is locked on a specific frequency and can also be used to generate precise frequencies with fine resolution.A PLL is a control system that generates a signal that has a fixed relation to the phase of a "reference" signal. A phase-locked loop circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. A phase-locked loop is an example of a control system using negative feedback.

PLL are widely used in radio, telecommunications, computers and other electronic applications. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital

logic designs such as microprocessors. Since a single integrated circuit can provide a complete PLL building block, the technique is widely used in modern electronic devices, with output frequencies from a fraction of a cycle per second up to many gigahertz.

4.3 STW8110x Multi-band RF frequency synthesizer with integrated VCOs

Based on the requirments of wideband RF front-end, we first choose STMicroelectronics STW8110x EVB as our fisrt LO to achieve variable center frequency. The STMicroelectronics STW8110x is an integrated RF synthesizer with two voltage controlled oscillators (VCOs). Showing high performance, high integration, low power, and multi-band performances,it featurs a fast settling time of 150 μs, which meets our demands best. at the same time, it covers a big frequency range from 625MHz to 5GHz.

- STMicroelectronics STW8110x Frequency Synthesizer.

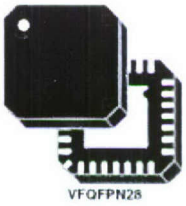


Figure 4.3: STMicroelectronics STW8110x frequency synthesizer.

STW81101:
3300 - 3900 MHz (direct output)
3800 - 4400 MHz (direct output)
1650 - 1950 MHz (internal divider by 2)
1900 - 2200 MHz (internal divider by 2)
825 - 975 MHz (internal divider by 4)
950 - 1100 MHz (internal divider by 4)

STW81102:
3000 - 3620 MHz (direct output)
4000 - 4650 MHz (direct output)
1500 - 1810 MHz (internal divider by 2)
2000 - 2325 MHz (internal divider by 2)
750 - 905 MHz (internal divider by 4)
1000 - 1162.5 MHz (internal divider by 4)

STW81103:
2500 - 3050 MHz (direct output)

4350 - 5000 MHz (direct output)
1250 - 1525 MHz (internal divider by 2)
2175 - 2500 MHz (internal divider by 2)
625 - 762.5 MHz (internal divider by 4)
1087.5 - 1250 MHz (internal divider by 4)

Excellent integrated phase noise
Fast lock time: 150 μs
Dual modulus programmable prescaler (16/17 or 19/20)
2 programmable counters to achieve a feedback division ratio from 256 to 65551(prescaler 16/17) and from 361 to 77836 (prescaler 19/20).
Programmable reference frequency divider (10 bits)
Phase frequency comparator and charge pump
Programmable charge pump current
Digital lock detector
Dual digital bus Interface: SPI and I2C bus witha 3-bit programmable address (1100A2A1A0)
3.3 V power supply
Power down mode (hardware and software)
Small size exposed pad VFQFPN28 package 5 x 5 x 1.0 mm
Process: BICMOS 0.35 μm SiGe

Frequency synthesizers form the basis of most radio designs and their performance largely affects the operation of the overall system. Requirements for signal-generating components in today's communications equipment include minimised phase noise and broadband frequency coverage.

To address these requirements, STW81103 exhibits the industry's best phase-noise performance for single-chip RF synthesizers, with measured values of 0.27 RMS (root mean square) at 1.16GHz, 0.6 RMS at 2.33GHz and 1.5 RMS at 4.67GHz with a frequency step of 200kHz. Outstanding suppression of random frequency fluctuations in a signal provides more design margin and the low phase noise also satisfies the stringent requirements of system manufacturers for minimised BER in voice and data transmission.

STW81103's embedded VCOs with automatic center-frequency calibration also provide outstanding multiband functionality. A single device spans frequency bands from 625-762.5MHz, 1,087.5-1,525MHz, 2,175-3,050MHz and 4,350-5,000MHz, allowing wireless system suppliers to use the device in wideband and multi-band applications. Among competing solutions, ST's family of integrated RF synthesizers needs just three devices (STW81101, STW81102 and STW81103) to cover the largest frequency range, from 625MHz to 5GHz.

Whereas existing solutions for microwave frequencies require discrete PLL devices and VCOs, the single-chip approach reduces both the BOMs and footprint by up to 70 percent. Other benefits of the monolithic synthesizer include an increase in device reliability and simplified supply chain for equipment manufacturers.

4.4 Some Other Available Products

For frequency synthesizer, the product available on market can support a large frequency range with a very fast switching speed. But most of such wideband frequency synthesizers are in big size, which are not proper for cognitive radio use, otherwise, some products have small size, but don't support fast switching speed.

With respect to switching speed, the Model 10512 VCO from Narda Microwave-East, INC. is the fastest one. Model 10512 employs two VCOs, While the tuning time for a single VCO is less than 100 ns, switching time between two retuned VCOs via the high-speed switch is less than 15 ns.

- Model 10512 VCO by Narda Microwave-East,INC.

Figure 4.4: Model 10512 by Narda Microwave-East,INC.

The standard Model 10512 has a frequency range of 2.8 to 3.2 GHz, but other frequencies can be accommodated well into the millimeter-wave region. It consumes only 11 W, measures 4 in. 4 in. x 0.6 in, weighs less than 1 oz,

With respect to wide output frequency range of frequency synthesizers or VCOs, the following is a glance of available products.

- Frequency synthesizer FSFS315555-500 by Synergy Microwave Corp.

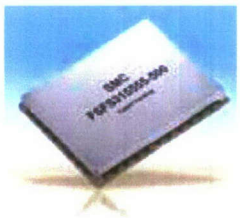


Figure 4.5: FSFS315555-500 by Synergy Microwave Corp.

The FSFS315555-500 features:

Frequency Range: 3150 to 5550 MHz.
Step Size: 5 MHz.
Settling Time: less than 50 μs.
Output Power: +5 dBm.
Pase Noise: -100 dBc/Hz (Typ.) offset @ 1 MHz Package Size: SMT package 1.0in x 1.25in.

- Frequency Synthesizers by Receiver Systems Division of Wide Band Systems,INC.

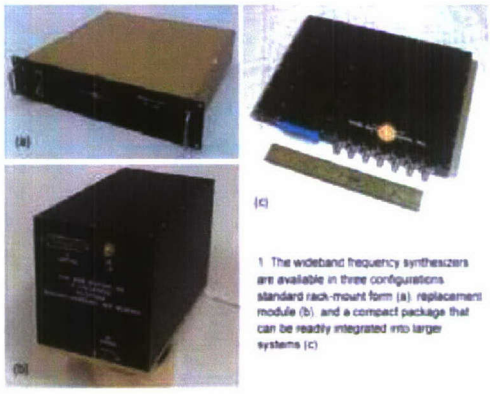


Figure 4.6: Frequency synthesizers by Wide Band Systems,INC.

Features:

Frequency Range: 2.0 to 18.0 GHz.
Switching Speed: 5 μs maximum (3 μs typical).
Frequency Resolution: as slow as 5.0 KHz.
Step Size: (12.7mm x 195mm x 135 mm).
Power Consumption: only 22W DC.

The output of this product can be a sequence of frequencies, a sequence of RF pulses, a sequence of amplitudes, or any combination of frequency, timing, and amplitude sequences desired.

- UFS 0.3-40 GHz Ultra Wide Band Frequency Synthesizer by Elcom,INC.

Features:

Frequency Range:
UFS-3: 0.3 to 3 GHz.
UFS-18: 0.3 to 18 GHz.

Figure 4.7: UFS 0.3-40 GHz Ultra Wideband frequency synthesizer.

Custom: 0.01 to 54 GHz.
Ultra-Fast Switching Speed: 250 ns, Full Band.
Frequency Resolution: 1 Hz resolution.
Low Phase Noise Floor: -150 dBc up to 20 GHz.
Low Phase Noise: -135 dBc 1 MHz offset @ 10 GHz.
Exceptionally Clean Signal: -68 dBc Spurious, -50 dBc Harmonics.

- PLL evaluation kit by Synergy Microwave Corp.

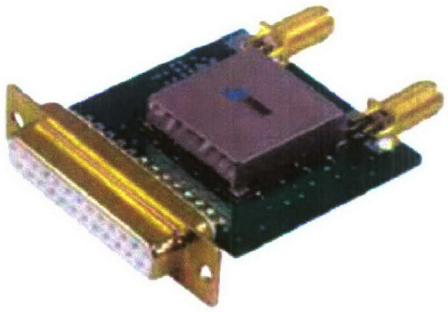


Figure 4.8: PLL evaluation kit by Synergy Microwave Corp.

Features:

Frequency Range: 2000 - 4000 MHz.
Step Size: 1000 kHz.
Settling Time: less than 8 ms.
Typical Phase Noise: -110 dbc/Hz @100 kHz

- Si4133 RF Synthesizer by Silicon Laboratories, Inc.

This Dual-band RF Synthesizers features:

Figure 4.9: Si4133 RF synthesizer by Silicon Laboratories, Inc.

RF1: 900 MHz to 1.8 GHz.
RF2: 750 MHz to 1.5 GHz.
IF Synthesizer: IF 62.5 MHz to 1.0 GHz.
Fast settling time:200 μs for GSM/DCS1800 applications.
Fully integrated VCO and programmable loop filters and Small-outline, 24-pin package (TSSOP).

Chapter 5

Signal Integrity

In our current transmitter, the main bottleneck lies in the connection between FPGA EVB board and DAC DK board. Since two boards are built individually, connection between them brings many problems. Firstly, the PCB layout of FPGA EVB is not designed for high speed data communications. When signal bandwidth is over 500 MHz, most of the LVDS I/O pairs generate distorted signals which are unusable for DAC. Only 7 pairs of I/O pairs were found on the FPGA EVB. The PCB layout of this FPGA EVB also causes synchronization problem. Since the usable pairs are not spread out on the board, their routing is not at same length and not synchronized. This causes the problem of DAC output at sampling rate over 500 Msps, which limits the maximum sampling rate of DAC. In addition, we found that the quality of the DAC board is not good even at lower sampling rate. The 3rd upper bit pair is always distorted. Therefore the output of the DAC is not reliable when utilizing 3 or more bits. As a result, only 2-bit quantization and 500 Msps sampling rate is used in the 14-bit 1 Gsps Fujistu DAC.

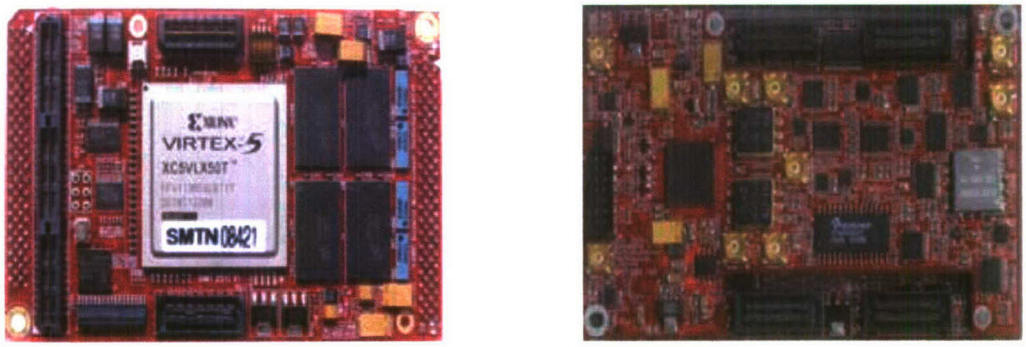
This connection problem limits the whole system performance. If FPGA and DAC connection is designed for maximized speed performance, this problem can be solved. A reasonable solution is to optimize FPGA and DAC interface. Due to the advances of current hardware industry, we have on-the-shelf products. Here we list our requirements and some typical products.

Requirements:

- Over 8-bit quantization resolution
- Over 1 Gsps sampling rate
- Dual channel analog DAC output for I/Q modulation
- High speed and high capacity FPGA
- Robust connections
- General I/Os

There are three categories of solutions satisfying our requirements: FPGA and DAC on independent boards, FPGA and DAC on one board and multiple FPGAs, DACs and ADCs. We will introduce each of them with an example.

Sundance



(a) Sundance base module SMT351 with Xilinx Virtex 5 (b) Sundance daughter module SMT381 with 14-bit 1 Gsps FPGA. This module can be connected to a variety of daughter DAC. It can be connected with the Virtex 5 base module. modules like DAC, ADC, etc.

Figure 5.1: Sundance base module and daughter module.

Sundance gives an independent-module solution. A base module with Virtex FPGA (Fig. 5.1(a)), a daughter module with DAC (Fig. 5.1(b))and a interface module. Robust data transmission between modules can be up to 1 GHz. Since FPGA and DAC are in different modules, the selection of FPGA types and DAC types is very flexible. The most advanced modules are SMT351T with Virtex 5 LX110T FPGA and SMT381 with dual channel 14-bit 1 Gsps DAC. Here are the main features of this solution:

- Dual channel 14-bit DAC (MB86064) sampling up to 1GHz
- Interface to FPGA Base Module via LVDS interface, using the Sundance Local Bus (SLB)
- Low-jitter system clock
- 50-Ohm analogue inputs and outputs, external triggers and clocks via MMBX (Huber and Suhner) connectors
- Virtex 5 LXT FPGA
- 4x SHB (160 I/O pins) connectors
- 2x 8-bit ComPorts for configurations
- Dual 16-bit differential bus with data rates up to 1GHz
- 1GB DDRII RAM per bank

Innovation Integration

The Innovation Integration TX VelociaPMC transmitter card (Fig. 5.2) has a 4 million gates Virtex II Pro FPGA and four 16-bit 1 Gsps DACs. With the four DACs, this board is good for multichannel DAC applications. However, the FPGA is Virtex II Pro, which is not the most advanced. This might limit the board's ability to handle applications requiring high speed and huge resource.

Features

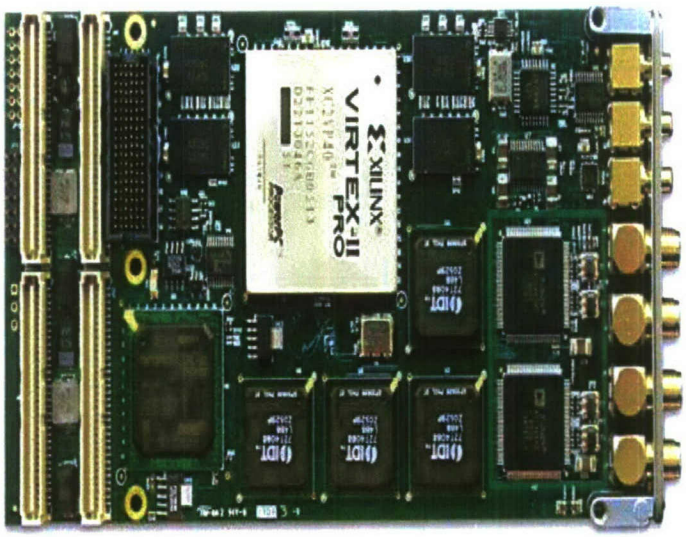


Figure 5.2: Innovation Integration TX VelociaPMC transmitter card. 4 million gates Virtex II and four 16-bit 1 Gsps DACs are on the board.

- Four AD9779, 16-bit, 1 GSPS DACs
- Virtex-II Pro FPGA, 4 Million gates
- PCI 64/66 with P4 port to host card
- 128MB SDRAM plus 2MB RAM for FPGA
- Low-jitter PLL clock source

Signumconcepts MAX SDR V2.1 PLATFORM

The idea of Signumconcepts MAX SDR V2.1 Platform (Fig. 5.3)is to provide multiple high speed A/D and D/A chips on one board. The purpose of this design is for software defined radio. Two on-board FPGAs are targeted for digital signal processing and data communication, respectively. The key features of this board are listed below:

- 2 Xilinx Virtex 4 SX55 User FPGAs
- 2 ADC channels 8 bits @ 3Gsps
- 2 DAC channels 12 bits @ 1.5Gsps
- 2 DAC channels 14 bits @ 160Msps
- Programmable and flexible clock scheme

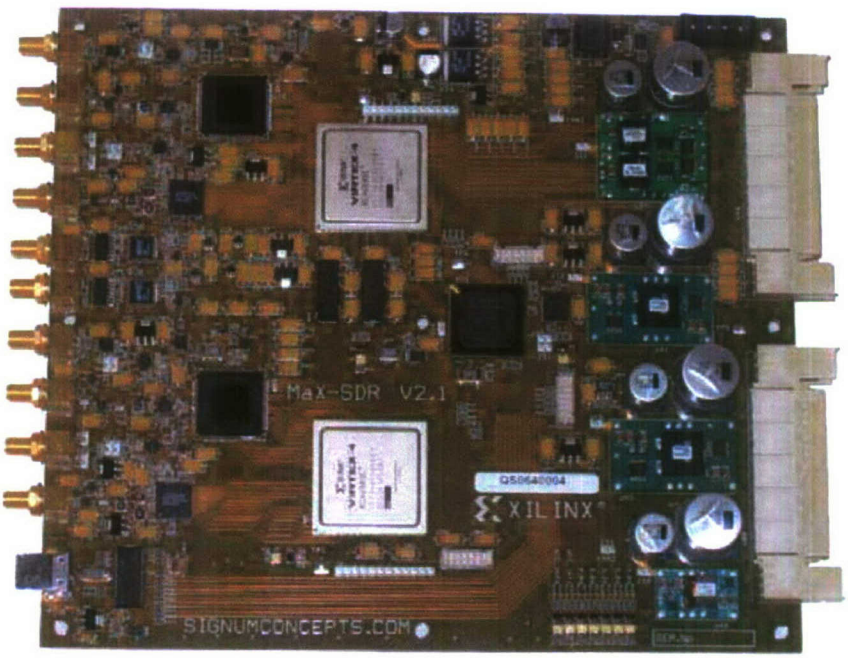


Figure 5.3: Signumconcepts MAX SDR Platform. There are two on-board Virtex 4 FPGAs and multiple ADCs and DACs.

Chapter 6

Spectral Efficiency for MIMO UWB System using Time Reversal

In this chapter, spectral efficiency for MIMO UWB system using time reversal is studied. In MIMO system, if fading is not considered, multiplexing gain and array gain will be introduced. We try to find optimal power allocation scheme for MIMO UWB system using time reversal to get spectral efficiency for this kind of system.

6.1 Multiplexing gain

It is assumed there are N_t transmitter antennas and N_r receiver antennas in the system. The channel transfer function is $\mathbf{H}(f)$ with bandwidth $W = f_1 - f_0$ where $f_0(> 0)$ is the starting frequency and $f_1(> 0)$ is the end frequency.

$$\mathbf{H}(f) = \begin{bmatrix} H_{11}(f) & H_{12}(f) & \cdots & H_{1N_t}(f) \\ H_{21}(f) & H_{22}(f) & \cdots & H_{2N_t}(f) \\ \vdots & \vdots & \vdots & \vdots \\ H_{N_r1}(f) & H_{N_r2}(f) & \cdots & H_{N_rN_t}(f) \end{bmatrix} \tag{6.1}$$

where $\mathbf{H}_{mn}(f)$ is the channel transfer function from the transmitter antenna n to the receiver antenna m. Its corresponding channel impulse response is

$$\mathbf{H}(t) = \begin{bmatrix} H_{11}(t) & H_{12}(t) & \cdots & H_{1N_t}(t) \\ H_{21}(t) & H_{22}(t) & \cdots & H_{2N_t}(t) \\ \vdots & \vdots & \vdots & \vdots \\ H_{N_r1}(t) & H_{N_r2}(t) & \cdots & H_{N_rN_t}(t) \end{bmatrix} \tag{6.2}$$

The spectrum-shaping filter in the transmitter side is

$$\mathbf{X}(t) = \begin{bmatrix} X_{11}(t) & X_{12}(t) & \cdots & X_{1N_r}(t) \\ X_{21}(t) & X_{22}(t) & \cdots & X_{2N_r}(t) \\ \vdots & \vdots & \vdots & \vdots \\ X_{N_t1}(t) & X_{N_t2}(t) & \cdots & X_{N_tN_r}(t) \end{bmatrix} \tag{6.3}$$

and its corresponding matrix transfer function is

$$\mathbf{X}(f) = \begin{bmatrix} X_{11}(f) & X_{12}(f) & \cdots & X_{1N_r}(f) \\ X_{21}(f) & X_{22}(f) & \cdots & X_{2N_r}(f) \\ \vdots & \vdots & \vdots & \vdots \\ X_{N_t1}(f) & X_{N_t2}(f) & \cdots & X_{N_tN_r}(f) \end{bmatrix} \tag{6.4}$$

The transmitted signal vector before the spectrum-shaping filter is $\mathbf{A}(t)$. The entries of $\mathbf{A}(t)$ are $A_1(t)$, $A_2(t)$,..., and $A_{N_r}(t)$,

$$\mathbf{A}(t) = \begin{bmatrix} A_1(t) \\ A_2(t) \\ \vdots \\ A_{N_r}(t) \end{bmatrix} \tag{6.5}$$

all of which are independent white Gaussian random processes with zero mean and unit PSD.

Let's define the $N_r \times N_r$ diagonal power allocation matrix $\mathbf{P}$,

$$\mathbf{P} = \begin{bmatrix} P_1 & & & \\ & P_2 & & \\ & & \ddots & \\ & & & P_{N_r} \end{bmatrix} \tag{6.6}$$

Thus, the transmitted signal at the transmitter array is

$$\mathbf{S}(t) = \mathbf{X}(t) * \left(\sqrt{\mathbf{P}}\mathbf{A}(t)\right) \tag{6.7}$$

where $*$ means convolution. The PSD matrix of the transmitted signals at the transmitter array is

$$\mathbf{R_S}(f) = \mathbf{X}(f)\mathbf{P}\mathbf{X}^H(f) \tag{6.8}$$

where H means conjugate transpose operator.

The received signal at the receiver array is

$$\mathbf{R}(t) = \mathbf{H}(t) * \mathbf{S}(t) + \mathbf{N}(t) \tag{6.9}$$

where $\mathbf{N}(t)$ is the additive white Gaussian noise the entries of which are independent random processes with zero mean and one-sided PSD N_0.

For time reversal scheme, it follows that

$$\mathbf{X}(f) = \mathbf{H}^H(f) \tag{6.10}$$

If one-sided situation is considered, then the total transmitted power is

$$\begin{aligned} P_t &= \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{R_S}\left(f\right)\right] df && (6.11)\\ &= \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{X}\left(f\right)\mathbf{P}\mathbf{X}^H\left(f\right)\right] df && (6.12)\\ &= \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{H}^H\left(f\right)\mathbf{P}\mathbf{H}\left(f\right)\right] df && (6.13)\\ &= \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{P}\mathbf{H}\left(f\right)\mathbf{H}^H\left(f\right)\right] df && (6.14) \end{aligned}$$

The spectral efficiency in this case is

$$\begin{aligned} \frac{C}{W} &= \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \frac{\mathbf{H}(f)\mathbf{R_S}(f)\mathbf{H}^H(f)}{N_0}\right) df}{f_1 - f_0} && (6.15)\\ &= \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \frac{\mathbf{H}(f)\mathbf{X}(f)\mathbf{P}\mathbf{X}^H(f)\mathbf{H}^H(f)}{N_0}\right) df}{f_1 - f_0} && (6.16)\\ &= \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \frac{\mathbf{H}(f)\mathbf{H}^H(f)\mathbf{P}\mathbf{H}(f)\mathbf{H}^H(f)}{N_0}\right) df}{f_1 - f_0} && (6.17)\\ &= \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \frac{\mathbf{P}\mathbf{H}(f)\mathbf{H}^H(f)\mathbf{H}(f)\mathbf{H}^H(f)}{N_0}\right) df}{f_1 - f_0} && (6.18) \end{aligned}$$

So the optimization problem can be described as

$$\begin{aligned} \max\ & \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \frac{\mathbf{P}\mathbf{H}(f)\mathbf{H}^H(f)\mathbf{H}(f)\mathbf{H}^H(f)}{N_0}\right) df}{f_1 - f_0}\\ s.t.\ & \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{P}\mathbf{H}\left(f\right)\mathbf{H}^H\left(f\right)\right] df \le P\\ & \mathbf{P} = \begin{bmatrix} P_1 & & & \\ & P_2 & & \\ & & \ddots & \\ & & & P_{N_r} \end{bmatrix}\\ & P = \rho N_0 \left(f_1 - f_0\right)\\ & P_i \ge 0,\ i = 1, 2, \ldots, N_r \end{aligned} \qquad (6.19)$$

where ρ is defined as the equivalent ratio of the transmitted signal power to the received noise power (TX SNR).

We want to solve the optimization problem 6.19 to get the optimal $P_i,\ i = 1, 2, \ldots, N_r$.

If $\beta_i = \int_{f_0}^{f_1} \left[\mathbf{H}\left(f\right)\mathbf{H}^H\left(f\right)\right]_{i,i} df,\ i = 1, 2, \ldots, N_r$ and equality constraint is considered, then $\sum_{i=1}^{N_r} \beta_i P_i = P$. If $\beta = [\beta_1\ \beta_2 \ldots \beta_{N_r}]$ and $\mathbf{p} = [P_1\ P_2 \ldots P_{N_r}]^T$, the equality constraint can be further simplified as $\beta\mathbf{p} = P$, where T means the transpose operator.

Define

$$\Psi\left(f\right) = \mathbf{H}\left(f\right)\mathbf{H}^H\left(f\right)\mathbf{H}\left(f\right)\mathbf{H}^H\left(f\right)/N_0 \qquad (6.20)$$

$$\Xi(f) = \mathbf{I}_{N_r}(f) + \mathbf{P}\Psi(f) \tag{6.21}$$

$$C_f(\mathbf{p}) = \log_{\mathbf{2}} \det(\mathbf{\Xi}(\mathbf{f})) \tag{6.22}$$

and

$$C(\mathbf{p}) = \int_{f_0}^{f_1} C_f(\mathbf{p})\, df \tag{6.23}$$

According to the concavity of $\log_2 \det(\bullet)$ and the affine transformation, $C_f(\mathbf{p})$ is concave in $P_i,\ i = 1, 2, \ldots, N_r$ [1]. Further more, $C(\mathbf{p})$ is also concave in $P_i,\ i = 1, 2, \ldots, N_r$.

According to the barrier method [1], $C_0(\mathbf{p})$ and $\phi(\mathbf{p})$ are defined as,

$$C_0(\mathbf{p}) = -C(\mathbf{p}) \tag{6.24}$$

and

$$\phi(\mathbf{p}) = -\sum_{i=1}^{N_r} \log(P_i(P - \beta_i P_i)) \tag{6.25}$$

Given strictly feasible $\mathbf{p}$, for example, $P_i,\ i = 1, 2, \ldots, N_r$ are set equally. $t > 0$, $\mu > 1$ and $\varepsilon > 0$. The optimal $\mathbf{p}$ can be obtained by the following iterative numerical method.

Repeat:

1 Computer $\mathbf{p}(t)$ by minimizing $f = tC_0 + \phi$, subject to $\beta\mathbf{p} = P$.

2 $\mathbf{p} := \mathbf{p}(t)$.

3 If $N_r/t < \varepsilon$, stop, else $t := \mu t$.

The newton method [1] can be used to solve the minimizing problem in the first step. $\Delta\mathbf{p}$ is defined as the Newton step at $\mathbf{p}$ and $\Delta\mathbf{p}$ can be characterized by

$$\begin{bmatrix} \nabla^2 f(\mathbf{p}) & \beta^T \\ \beta & 0 \end{bmatrix} \begin{bmatrix} \Delta\mathbf{p} \\ w \end{bmatrix} = \begin{bmatrix} -\nabla f(\mathbf{p}) \\ 0 \end{bmatrix} \tag{6.26}$$

where

$$\nabla f(\mathbf{p}) = [\frac{\partial f(\mathbf{p})}{\partial P_1} \ \frac{\partial f(\mathbf{p})}{\partial P_2} \cdots \frac{\partial f(\mathbf{p})}{\partial P_{N_r}}]^T \tag{6.27}$$

and

$$\nabla^2 f(\mathbf{p}) = \begin{bmatrix} \frac{\partial^2 f(\mathbf{p})}{\partial P_1 \partial P_1} & \frac{\partial^2 f(\mathbf{p})}{\partial P_1 \partial P_2} & \cdots & \frac{\partial^2 f(\mathbf{p})}{\partial P_1 \partial P_{N_r}} \\ \frac{\partial^2 f(\mathbf{p})}{\partial P_2 \partial P_1} & \frac{\partial^2 f(\mathbf{p})}{\partial P_2 \partial P_2} & \cdots & \frac{\partial^2 f(\mathbf{p})}{\partial P_2 \partial P_{N_r}} \\ \vdots & \vdots & \vdots & \vdots \\ \frac{\partial^2 f(\mathbf{p})}{\partial P_{N_r} \partial P_1} & \frac{\partial^2 f(\mathbf{p})}{\partial P_{N_r} \partial P_2} & \cdots & \frac{\partial^2 f(\mathbf{p})}{\partial P_{N_r} \partial P_{N_r}} \end{bmatrix} \tag{6.28}$$

$\partial f(\mathbf{p})/\partial P_i,\ i = 1, 2, \ldots, N_r$ is derived as,

$$\partial f(\mathbf{p})/\partial P_i = -t \int_{f_0}^{f_1} \frac{\sum_{m=1}^{N_r} (-1)^{i+m} [\Psi(f)]_{i,m} \det\left([\Xi(f)]_{i,m,\text{sub}}\right)}{\det(\Xi(f)) \log 2} df - \frac{P - 2\beta_i P_i}{P_i(P - \beta_i P_i)} \tag{6.29}$$

where $[\Xi(f)]_{i,m,\text{sub}}$ is the sub-matrix which is obtained from $\Xi(f)$ when the entries in the ith row and the mth column are removed.

If $i=j,\ i=1,2,\ldots,N_r, j=1,2,\ldots,N_r$, then $\frac{\partial^2 f(\mathbf{p})}{\partial P_i \partial P_j}$ is derived as,

$$\frac{\partial^2 f(\mathbf{p})}{\partial P_i \partial P_j} = t\int_{f_0}^{f_1} \frac{\left(\sum_{m=1}^{N_r}(-1)^{i+m}[\Psi(f)]_{i,m}\det\left([\Xi(f)]_{i,m,\text{sub}}\right)\right)^2}{\det^2(\Xi(f))\log 2}df - g_1 \tag{6.30}$$

where g_1 is equal to

$$g_1 = \frac{2\beta_i P_i P - 2\beta_i^2 P_i^2 - P^2}{P_i^2(P-\beta_i P_i)^2} \tag{6.31}$$

If $i\neq j,\ i=1,2,\ldots,N_r, j=1,2,\ldots,N_r$, then $\frac{\partial^2 f(\mathbf{p})}{\partial P_i \partial P_j}$ is derived as,

$$\frac{\partial^2 f(\mathbf{p})}{\partial P_i \partial P_j} = -t\int_{f_0}^{f_1} \frac{\mathrm{T}(f)}{\det^2(\Xi(f))\log 2}df \tag{6.32}$$

where $\mathrm{T}(f)$ is equal to

$$\begin{array}{l}\det(\Xi(f))\sum_{m=1}^{N_r}\left((-1)^{i+m}[\Psi(f)]_{i,m}\frac{\left(\det\left([\Xi(f)]_{i,m,\text{sub}}\right)\right)}{\partial P_j}\right)\\ -\frac{\partial(\det([\Xi(f)]))}{\partial P_j}\sum_{m=1}^{N_r}(-1)^{i+m}[\Psi(f)]_{i,m}\det\left([\Xi(f)]_{i,m,\text{sub}}\right)\end{array} \tag{6.33}$$

If $j>i$, then $\partial\left(\det\left([\Xi(f)]_{i,m,\text{sub}}\right)\right)\Big/\partial P_j$ is equal to

$$\begin{array}{l}\sum_{n=1}^{m-1}(-1)^{j-1+n}[\Psi(f)]_{j,n}\det\left(\left([\Xi(f)]_{i,m,\text{sub}}\right)_{j-1,n,\text{sub}}\right)\\ +\sum_{n=m+1}^{N_r}(-1)^{j-1+n-1}[\Psi(f)]_{j,n}\det\left(\left([\Xi(f)]_{i,m,\text{sub}}\right)_{j-1,n-1,\text{sub}}\right)\end{array} \tag{6.34}$$

If $j<i$, then $\partial\left(\det\left([\Xi(f)]_{i,m,\text{sub}}\right)\right)\Big/\partial P_j$ is equal to

$$\begin{array}{l}\sum_{n=1}^{m-1}(-1)^{j+n}[\Psi(f)]_{j,n}\det\left(\left([\Xi(f)]_{i,m,\text{sub}}\right)_{j,n,\text{sub}}\right)\\ +\sum_{n=m+1}^{N_r}(-1)^{j+n-1}[\Psi(f)]_{j,n}\det\left(\left([\Xi(f)]_{i,m,\text{sub}}\right)_{j,n-1,\text{sub}}\right)\end{array} \tag{6.35}$$

$\partial(\det([\Xi(f)]))/\partial P_j$ is equal to

$$\partial(\det([\Xi(f)]))/\partial P_j = \sum_{m=1}^{N_r}(-1)^{j+m}[\Psi(f)]_{j,m}\det\left([\Xi]_{j,m,\text{sub}}\right) \tag{6.36}$$

6.2 Array gain

If we only want to exploit the array gain of MIMO system, then the transmitted signal before the precoding matrix filter is $\mathbf{A}(t)$ and $\mathbf{A}(t)$ is expressed as

$$\mathbf{A}(t) = \mathbf{L}A(t) \tag{6.37}$$

where $A(t)$ is the white Gaussian random process with zero mean and unit PSD. $\mathbf{L}$ can be similarly treated as the power allocation vector,

$$\mathbf{L} = \begin{bmatrix} L_1 \\ L_2 \\ \vdots \\ L_{N_r} \end{bmatrix} \tag{6.38}$$

Thus, the transmitted signal at the transmitter array is

$$\mathbf{S}(t) = \mathbf{X}(t) * \mathbf{A}(t) \tag{6.39}$$

$$= \mathbf{X}(t) * (\mathbf{L}A(t)) \tag{6.40}$$

and the PSD matrix of the transmitted signals at the transmitter array is

$$\mathbf{R_S}(f) = \mathbf{X}(f)\mathbf{L}\mathbf{L}^T\mathbf{X}^H(f) \tag{6.41}$$

For time reversal scheme, it follows that

$$\mathbf{X}(f) = \mathbf{H}^H(f) \tag{6.42}$$

If one-sided situation is considered, then the total transmitted power is

$$P_t = \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{R_S}(f)\right]df \tag{6.43}$$

$$= \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{X}(f)\mathbf{L}\mathbf{L}^T\mathbf{X}^H(f)\right]df \tag{6.44}$$

$$= \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{H}^H(f)\mathbf{L}\mathbf{L}^T\mathbf{H}(f)\right]df \tag{6.45}$$

$$= \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{L}\mathbf{L}^T\mathbf{H}(f)\mathbf{H}^H(f)\right]df \tag{6.46}$$

The spectral efficiency in this case is

$$\frac{C}{W} = \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \frac{\mathbf{H}(f)\mathbf{R_S}(f)\mathbf{H}^H(f)}{N_0}\right)df}{f_1 - f_0} \tag{6.47}$$

$$= \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \frac{\mathbf{H}(f)\mathbf{X}(f)\mathbf{L}\mathbf{L}^T\mathbf{X}^H(f)\mathbf{H}^H(f)}{N_0}\right)df}{f_1 - f_0} \tag{6.48}$$

$$= \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \frac{\mathbf{H}(f)\mathbf{H}^H(f)\mathbf{L}\mathbf{L}^T\mathbf{H}(f)\mathbf{H}^H(f)}{N_0}\right)df}{f_1 - f_0} \tag{6.49}$$

$$= \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \frac{\mathbf{L}\mathbf{L}^T\mathbf{H}(f)\mathbf{H}^H(f)\mathbf{H}(f)\mathbf{H}^H(f)}{N_0}\right)df}{f_1 - f_0} \tag{6.50}$$

So the optimization problem can be described as

$$\begin{aligned} \max \quad & \frac{\int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f)+\frac{\mathbf{L}\mathbf{L}^T\mathbf{H}(f)\mathbf{H}^H(f)\mathbf{H}(f)\mathbf{H}^H(f)}{N_0}\right) df}{f_1-f_0} \\ s.t. \quad & \int_{f_0}^{f_1} \mathbf{tr}\left[\mathbf{L}\mathbf{L}^T\mathbf{H}(f)\mathbf{H}^H(f)\right] df \le P \\ & \mathbf{L} = \begin{bmatrix} L_1 \\ L_2 \\ \vdots \\ L_{N_r} \end{bmatrix} \\ & P = \rho N_0 (f_1 - f_0) \\ & L_i \ge 0,\ i = 1, 2, \ldots, N_r \end{aligned} \tag{6.51}$$

We want to solve the optimization problem 6.51 to get the optimal $L_i,\ i = 1, 2, \ldots, N_r$.

Similarly, let $\Psi(f) = \mathbf{H}(f)\mathbf{H}^H(f)\mathbf{H}(f)\mathbf{H}^H(f)/N_0$ and $\Upsilon(f) = \mathbf{H}(f)\mathbf{H}^H(f)$. Define,

$$C(\mathbf{L}) = \int_{f_0}^{f_1} \log_2 \det\left(\mathbf{I}_{N_r}(f) + \mathbf{L}\mathbf{L}^T\Psi(f)\right) df \tag{6.52}$$

$$= \int_{f_0}^{f_1} \log_2\left(1 + \mathbf{L}^T\Psi(f)\mathbf{L}\right) df \tag{6.53}$$

and

$$h(\mathbf{L}) = \int_{f_0}^{f_1} \left(\mathbf{L}^T\Upsilon(f)\mathbf{L}\right) df - P \tag{6.54}$$

The first derivative $C(\mathbf{L})$ and $h(\mathbf{L})$ are shown below,

$$\nabla C(\mathbf{L}) = -\int_{f_0}^{f_1} \frac{\left(\Psi(f) + \Psi^T(f)\right)\mathbf{L}}{\left(1 + \mathbf{L}^T\Psi(f)\mathbf{L}\right)\log 2} df \tag{6.55}$$

and

$$\nabla h(\mathbf{L}) = \left(\int_{f_0}^{f_1} \left(\Upsilon(f) + \Upsilon^T(f)\right) df\right)\mathbf{L} \tag{6.56}$$

The second derivative $C(\mathbf{L})$ and $h(\mathbf{L})$ are shown below,

$$\nabla^2 C(\mathbf{L}) = \int_{f_0}^{f_1} \frac{\left(\Psi(f) + \Psi^T(f)\right)\left(1 + \mathbf{L}^H\Psi(f)\mathbf{L}\right) - \left(\Psi(f) + \Psi^T(f)\right)\mathbf{L}\mathbf{L}^T\left(\Psi(f) + \Psi^T(f)\right)}{\left(1 + \mathbf{L}^T\Psi(f)\mathbf{L}\right)^2 \log 2} df \tag{6.57}$$

and

$$\nabla h^2(\mathbf{L}) = \int_{f_0}^{f_1} \left(\Upsilon(f) + \Upsilon^T(f)\right) df \tag{6.58}$$

Even though the first and second derivatives of the objective function and constraint function can be easily derived, because the objective function is a nonlinear and nonconvex function, it is hard to use deterministic algorithm to solve the optimization problem 6.51. In recently years, the random algorithm is widely used to solve the nonlinear and nonconvex optimization problem to get the near optimal solution. Here the particle swarm optimization (PSO) is employed to solve the optimization problem 6.51.

PSO is a swarm intelligence based algorithm to find a solution to an optimization problem in a search space [2]. There are many particles which have a position and a velocity in the swarm. In a maximization optimization problem, best simply meaning the position with the largest objective value. Particles in a swarm communicate good positions to each other and adjust their own position and velocity based on these good positions [2]. So a particle has the following information to make a suitable change in its position and velocity: (1) a global best that is known to all and immediately updated when a new best position is found by any particle in the swarm; (2) the local best, which is the best solution that the particle has seen [2].

Suppose there are N particles in N_r-dimensional space. After K iterations, the algorithm is stopped. When the kth iteration begins, the position of particle i is $\mathbf{L}_i^{k-1}$. The velocity of particle i is $\mathbf{V}_i^{k-1}$. The local best position of particle i is

$$\mathbf{L}_{i\text{best}}^{k} = \max_{\left\{\mathbf{L}_{i\text{best}}^{k-1}, \mathbf{L}_i^{k-1}\right\}} C\left(\mathbf{L}\right) \tag{6.59}$$

The global best position is

$$\mathbf{L}_{\text{gbest}}^{k} = \max_{\left\{\mathbf{L}_{i\text{best}}^{k},\, i=1,2,\ldots,N\right\}} C\left(\mathbf{L}\right) \tag{6.60}$$

Then the velocity of particle i in the kth iteration is

$$\mathbf{V}_i^k = w \times \mathbf{V}_i^{k-1} + c_1 \times \text{rand} \times \left(\mathbf{L}_{i\text{best}}^{k} - \mathbf{L}_i^{k-1}\right) + c_2 \times \text{rand} \times \left(\mathbf{L}_{\text{gbest}}^{k} - \mathbf{L}_i^{k-1}\right) \tag{6.61}$$

and the new position of particle i is $\mathbf{L}_i^k = \mathbf{L}_i^{k-1} + \mathbf{V}_i^k$. Where rand means random value drawn from a uniform distribution on the unit interval; w is the inertia weight; c_1 and c_2 are two positive constants, called the cognitive and social parameter respectively.

Meanwhile, if $h\left(\mathbf{L}_i^k\right) > 0$, that means the particle i moves to the infeasible position, then $C\left(\mathbf{L}_i^k\right)$ is set extremely small value. Although PSO algorithm can not guarantee the optimal solution, it still can find the near optimal solution which also gives the fundamental limit of the system from spectral efficiency's point of view.

6.3 Results

The numerical results of spectral efficiency will be presented in this section. 3-by-3 UWB channel transfer function is measured according to the description in [3]. In the barrier method, t is initially set 1. μ is set 2 and ε is set 0.00000001. In PSO algorithm, the number of particles in the swarm is 200 and the number of iterations is 150. w is set $\frac{\text{rand}}{2} + 0.5$. $c_1 = c_2 = 2$. Fig. 6.1 shows the spectral efficiencies for MIMO UWB system using time reversal. Fig. 6.2 shows the ratio of spectral efficiency of array gain to that of multiplexing gain. In the high SNR region, the spectral efficiency of multiplexing gain is obviously larger than that of array gain. While in the low SNR region, the spectral efficiency of multiplexing gain is almost the same as that of array gain.

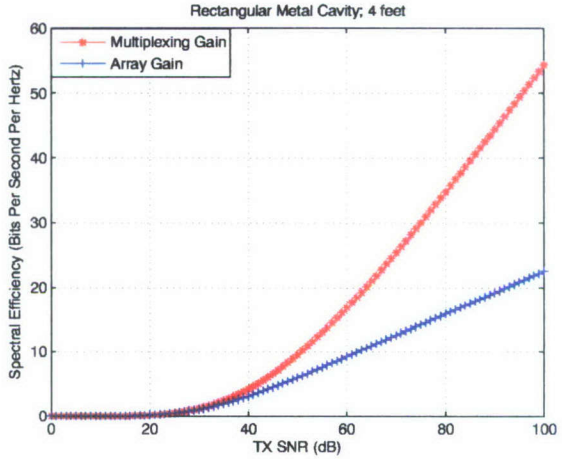


Figure 6.1: Spectral efficiencies for MIMO UWB system using time reversal.

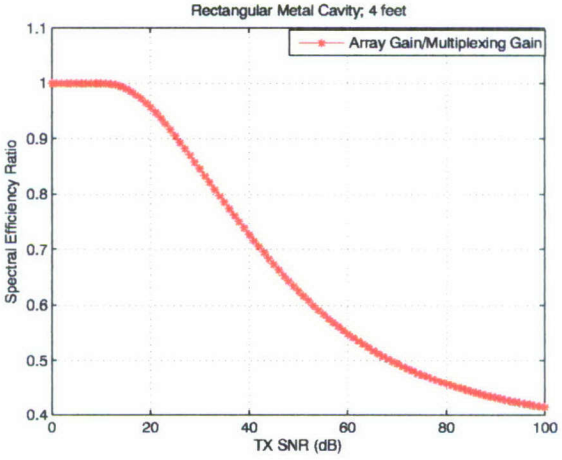


Figure 6.2: The ratio of spectral efficiency of array gain to that of multiplexing gain.

Bibliography

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